REMARKS

Reconsideration of this application, as presently amended, is respectfully requested. Claims 1-20 are pending in this application. Claims 16 and 20 stand rejected. Claims 1-12 were withdrawn from consideration as being drawn to a non-elected invention. Finally, claims 13-15 and 17-19 were indicated to be allowable if rewritten to overcome the objections set forth in the Office Action. Claims 13-15 and 17-19 should be in now be condition for allowance as a result of the present amendments to these claims.

Request to Withdraw Finality of Office Action

It is respectfully submitted that the finality of the current Office Action should be withdrawn because a new ground of rejection has been introduced that was not necessitated by applicant's amendment of the claims.

More specifically, as set forth in the Manual of Patenting Examining Procedure (MPEP) §706.07(a), "Under present practice, second or any subsequent actions on the merits shall be final, except where the Examiner introduces a new ground of rejection that is neither necessitated by Applicant's amendment of the claims nor based on information submitted in an Information Disclosure Statement filed during the period set forth in 37 CFR § 1.97(c) with the fee set forth in 37 CFR §1.17(p)".

It is submitted that the rejection of claims 16 and 20 under 35 U.S.C. §112, second paragraph, is a new ground of rejection that was not necessitated by Applicant's amendment of the claims and is asserted for the first time in the final Office Action. None of the claims were

amended in the previous response filed August 31, 2005. Accordingly, under the guidelines of the MPEP §706.07(a), the final rejection is premature and should be withdrawn. Withdrawal of the finality of the present Office Action is respectfully requested.

Claim Objections

Claims 13 and 17 were objected to for informalities. More specifically, the Office Action asserts that the recitation "said computed values" should be changed to --the computed values-- in claims 13 and 17 in order to avoid lack of antecedent basis.

It is noted that claims 13 and 17 recite both "said computed values" and "the computed values". To obviate the objection, claims 13 and 17 have been amended such that terminology is used consistently throughout. Specifically, "the computed values" in claim 13, line 16 has been changed to --said computed values--. This change is consistent with the two other instances of "said computed values" in the claim. Claim 17 has been amended in the same manner as claim 13.

In view of the above amendments, it is submitted that the objection to claims 13 and 17 is overcome and should be withdrawn.

Claim Rejections – 35 U.S.C. §112, second paragraph

Claims 16 and 20 were rejected under 35 U.S.C. §112, second paragraph, for alleged indefiniteness. Specifically, the Office Action asserts that the language "said sequence of scrambling codes" and "said obtained matrix" in each of claims 16 and 20 lacks antecedent basis.

Claims 16 and 20 have been amended such that the terminology objected to by the Examiner has appropriate antecedent basis.

In view of the above amendments, reconsideration and withdrawal of the rejection under §112, second paragraph, are respectfully requested.

Claim Rejections – 35 U.S.C. §102

Claims 16 and 20 were rejected under 35 U.S.C. §102(a) as being anticipated by Applicants' admitted prior art (**AAPA**). For the reasons set forth in detail below, this rejection is respectfully traversed.

The current Office Action repeats the same rejection set forth in the previous Office Action mailed June 1, 2005. Therefore, the remarks below focus on the Examiner's "*Response to Arguments*" set forth on pages 2 and 3, Item 1 of the Office Action.

In the Response filed on August 31, 2005, it was argued that the shift registers 11, 12, 13 and 14 shown in the **AAPA** (Fig. 16 of the present application), and considered by the Examiner to correspond to the claimed "logic circuit," do not function in the same manner as the claimed logic circuit. It was also argued that the claimed "arithmetic circuit" does not operate in the same manner as the arithmetic circuit shown in Fig. 16.

In the "*Response to Arguments*," the Examiner asserts that the shift registers 11-14, selectors 15-18 and exclusive OR circuit 20 is a logic circuit. The Examiner notes that the registers 11-14 are set with inputs D_3-D_0 that can be represented as a matrix (see e.g., page 6, line 20 of applicant's specification). The Examiner also notes that the circuit consisting of shift

registers 11-14, selectors 15-18 and exclusive OR circuit 20 outputs a sequence of scrambling codes. See Office Action, page 2, lines 17-22.

The Examiner is permitted to give the claim language its broadest reasonable interpretation. Therefore, it may be reasonable for the Examiner to interpret the circuit consisting of shift registers 11-14, selectors 15-18 and exclusive OR circuit 20 as "obtaining by a predetermined operation a matrix to determine a value of each code forming a sequence of scrambling codes" (inputs D_3-D_0 can be represented as a matrix and are obtained by a shift operation, and inputs D_3-D_0 are used to generate a sequence of scrambling codes).

However, even if the claim language regarding the "logic circuit" is given its broadest reasonable interpretation, the **AAPA** does not disclose or suggest the claimed "arithmetic circuit." More specifically, the claimed ***"arithmetic circuit"*** *multiplies* ***"predetermined initial values"*** stored in a storage circuit by ***"said [obtained] matrix."***

In contrast to the claimed invention, as shown in Fig. 16 the arithmetic circuit 21 multiplies predetermined initial values Ri = Ri_3-Ri_0 stored in initial value buffer 22 by matrixes $M_{3(100)}$, $M_{2(100)}$, $M_{1(100)}$, $M_{0(100)}$ that are obtained and stored in advance (see page 9, lines 7-9 of Applicant's specification). However, the predetermined initial values Ri = Ri_3-Ri_0 are **not** multiplied by a matrix obtained by a predetermined operation of the circuit consisting of shift registers 11-14, selectors 15-18 and exclusive OR circuit 20 (considered to correspond to the claimed "logic circuit").

Accordingly, unlike the claimed "arithmetic circuit," the arithmetic circuit 21 in the **AAPA** does not multiply predetermined initial values by a matrix obtained by a predetermined operation of a logic circuit.

A rejection under §102 requires that each and every element recited in the claims must be disclosed in the prior art reference exactly as claimed. As discussed above, **AAPA** does not disclose each and every element recited in claim 16. Claim 20 recites the same elements as claim 16 (i.e., storage circuit, logic circuit, arithmetic circuit) and is allowable for the same reasons discussed above with respect to claim 16.

In view of the above remarks, it is respectfully submitted that the rejection under §102 is improper and should be withdrawn. Accordingly, reconsideration and withdrawal of the rejection under §102 are respectfully requested.

CONCLUSION

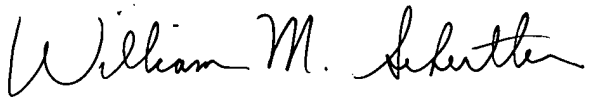
In view of the foregoing amendments and accompanying remarks, it is submitted that all pending claims are in condition for allowance. A prompt and favorable reconsideration of the rejection and an indication of allowability of all pending claims are earnestly solicited.

If the Examiner believes that there are issues remaining to be resolved in this application, the Examiner is invited to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite and complete prosecution of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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